the same process as the cell transistors;

forming gate insulating films of said select transistors on the exposed surface of the substrate; and

forming the control gate electrodes of said cell transistors and forming gate electrodes of said select transistors on said gate insulating films.

2. (Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising:

A1 cont.

simultaneously forming a first diffused layer serving as source and drain regions of said cell transistors and a second diffused layer serving as source and drain regions of said select transistors.

3. (Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

4. (Amended) The method of manufacturing a semiconductor memory device according to claim 2, further comprising:

forming gate insulating films of transistors of a peripheral circuit comprising a